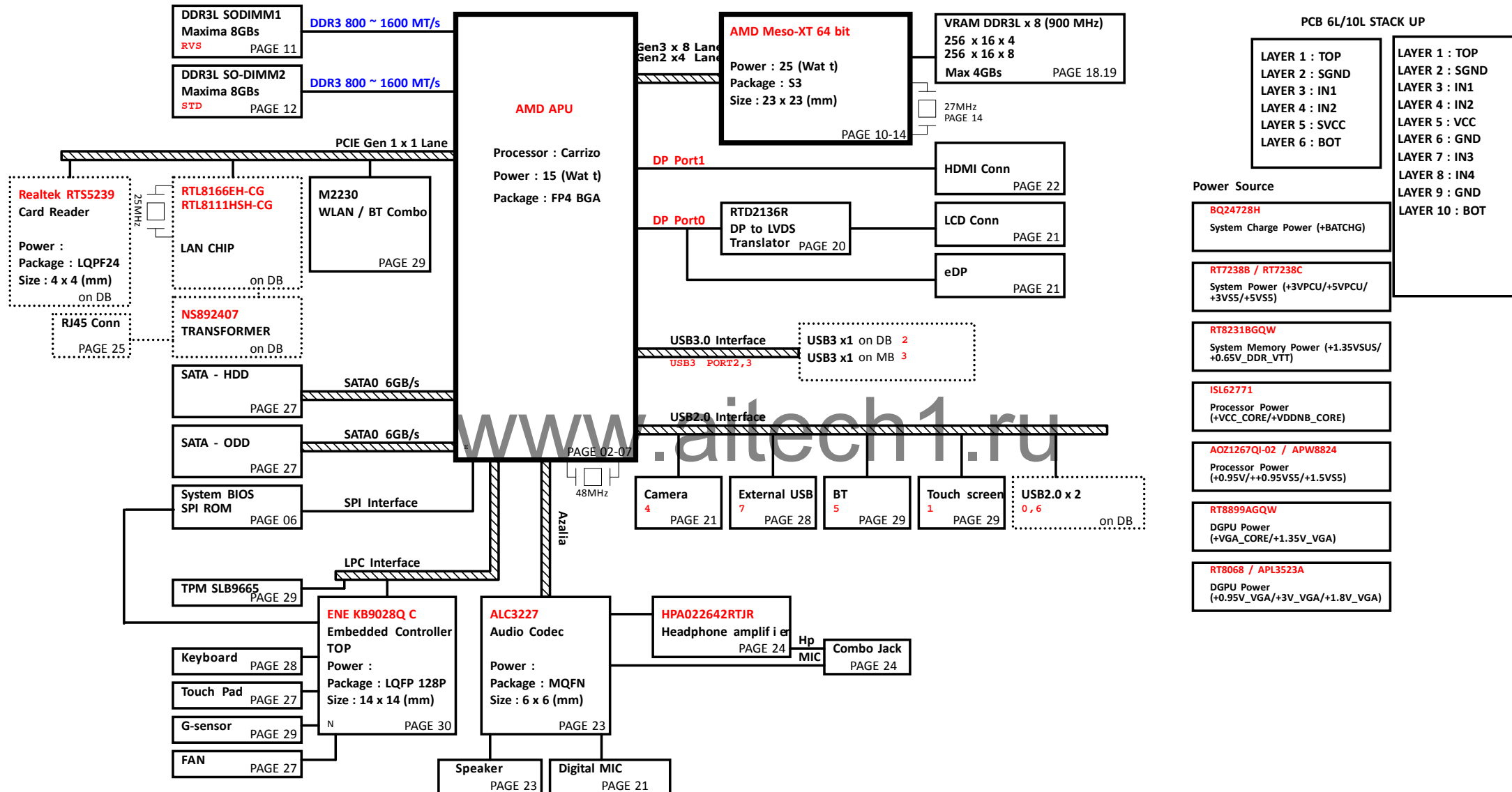


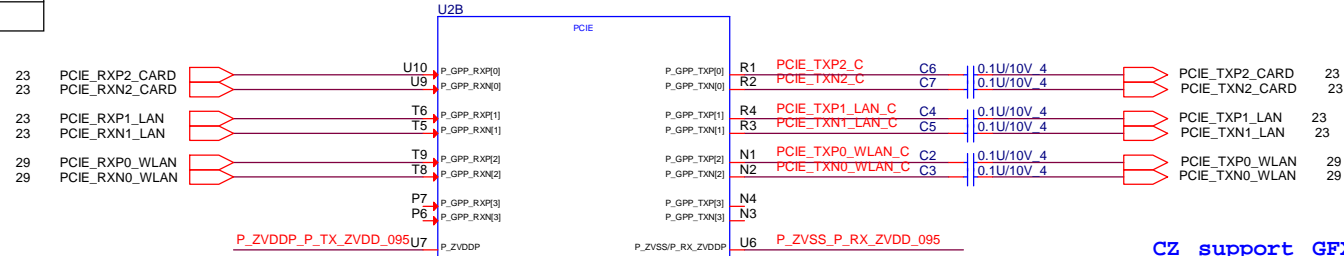
Chocolate_AMD Carrizo(L) DIS/UMA (14.0"/15.6"/17.3")

01



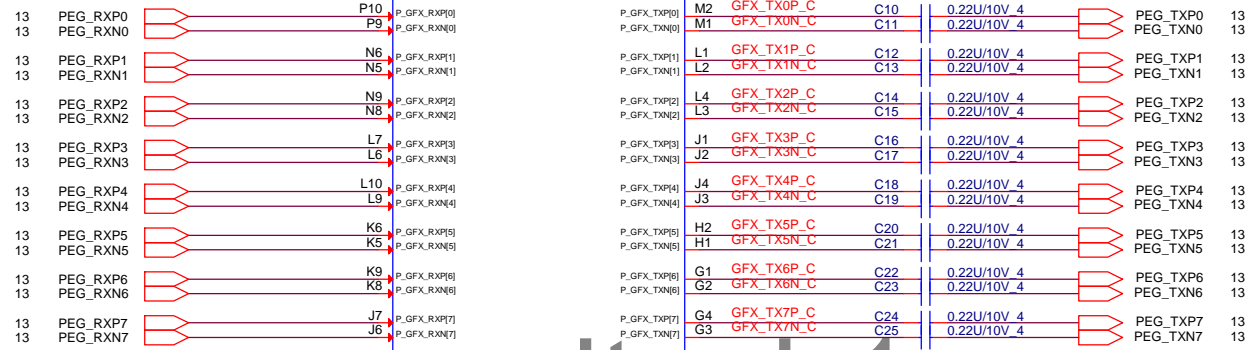
	QBCON	TOPBSQ
Carrizo	AJ1802CUT01	AJ1802CUT02

Carrizo DB phase use AJ1802CUT00



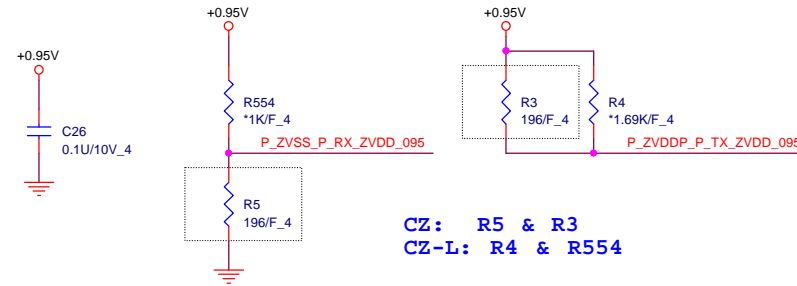
CZ support GFX 0~7 & Gen3

CZ-L only support GFX 0~3 & Gen2



Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

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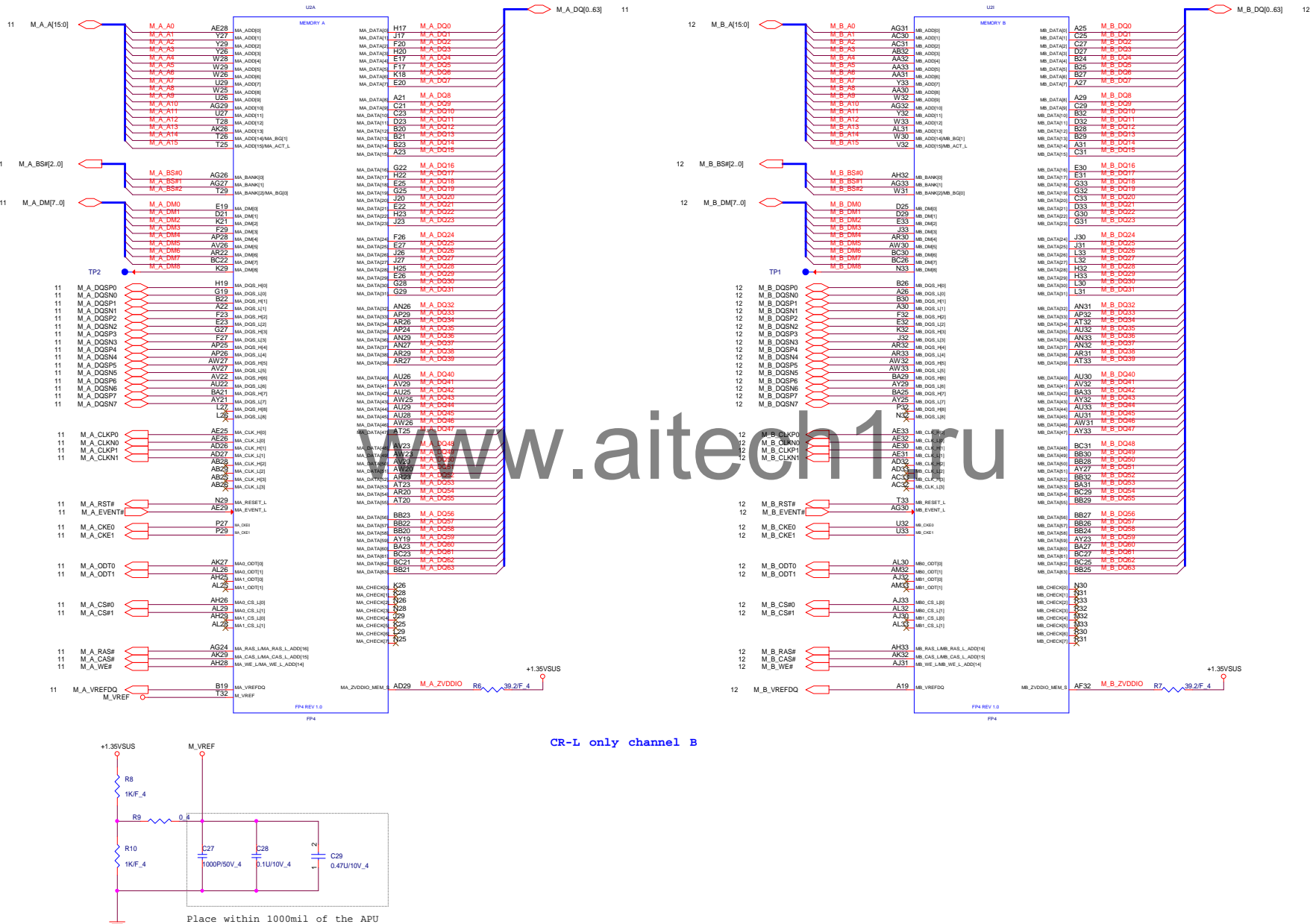


CZ: R5 & R3
CZ-L: R4 & R554



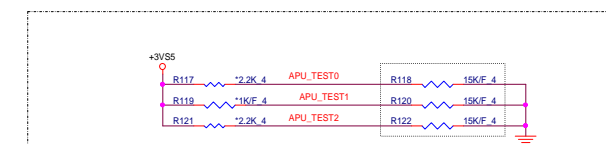
PROJECT : X21
Quanta Computer Inc.

Size	Document Number	Rev
	Carrizo 1/7 (PCIe)	1A
Date: Friday, October 17, 2014	Sheet	of 43

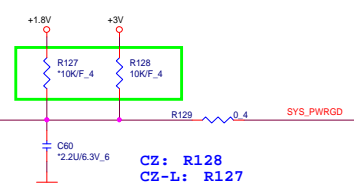


05

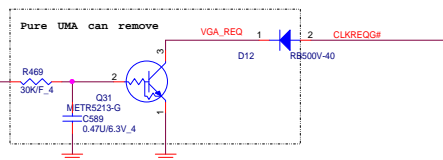
Board ID [7:6]	Definition
00	Reserve



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted. FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only yuba JTAG enabled



CZ: R128
CZ-L: R127

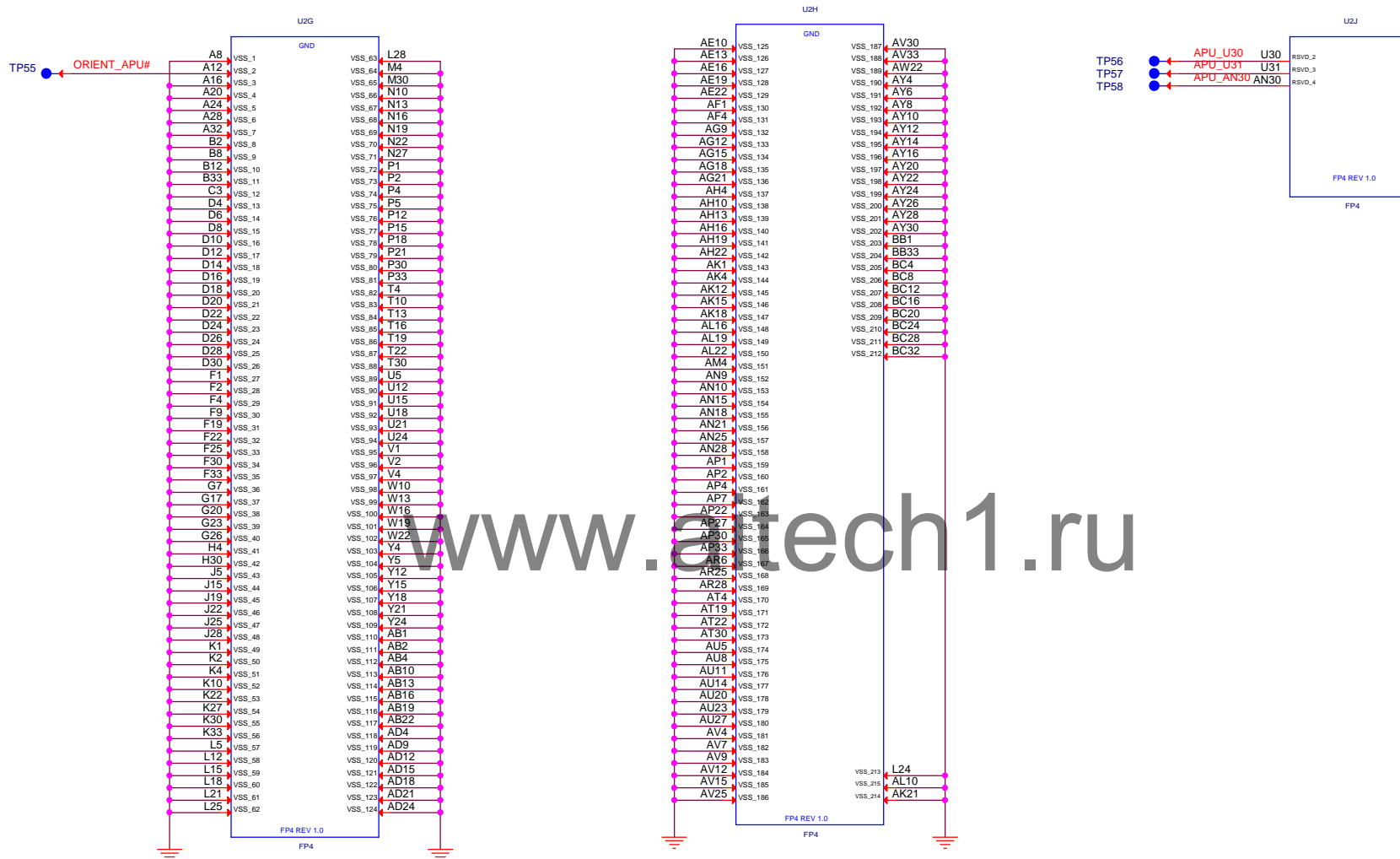




28 Right side USB Combo 3.0/2.0.

30	EC_SPI_WP_R	EC_SPI_WP_R
30	EC_BIOS_CS#	EC_BIOS_CS#
30	EC_BIOS_SPI_CLK_I	EC_BIOS_SPI_CLK_I
30	EC_BIOS_WR#	EC_BIOS_WR#
30	EC_BIOS_RD#	EC_BIOS_RD#

Size	Document Number	Rev
	Carrizo 5/7 (SATA/USB/SPI)	1A

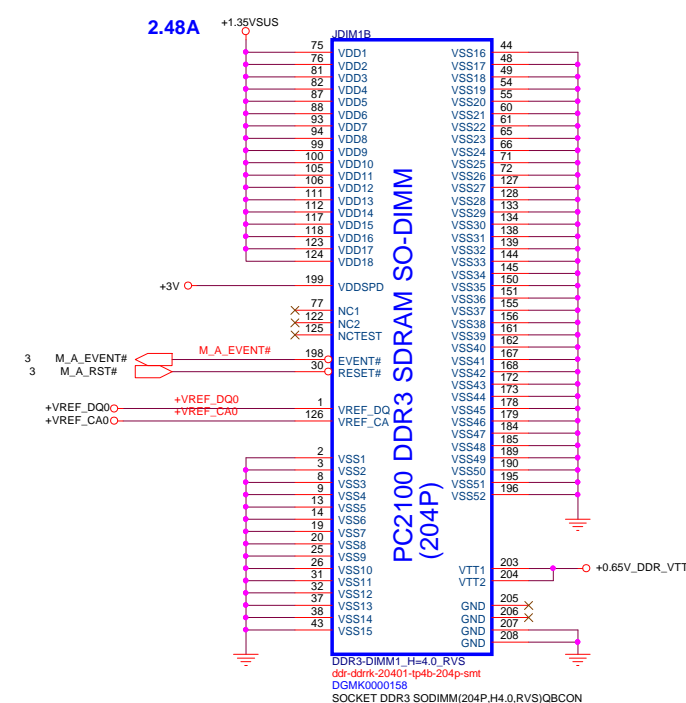
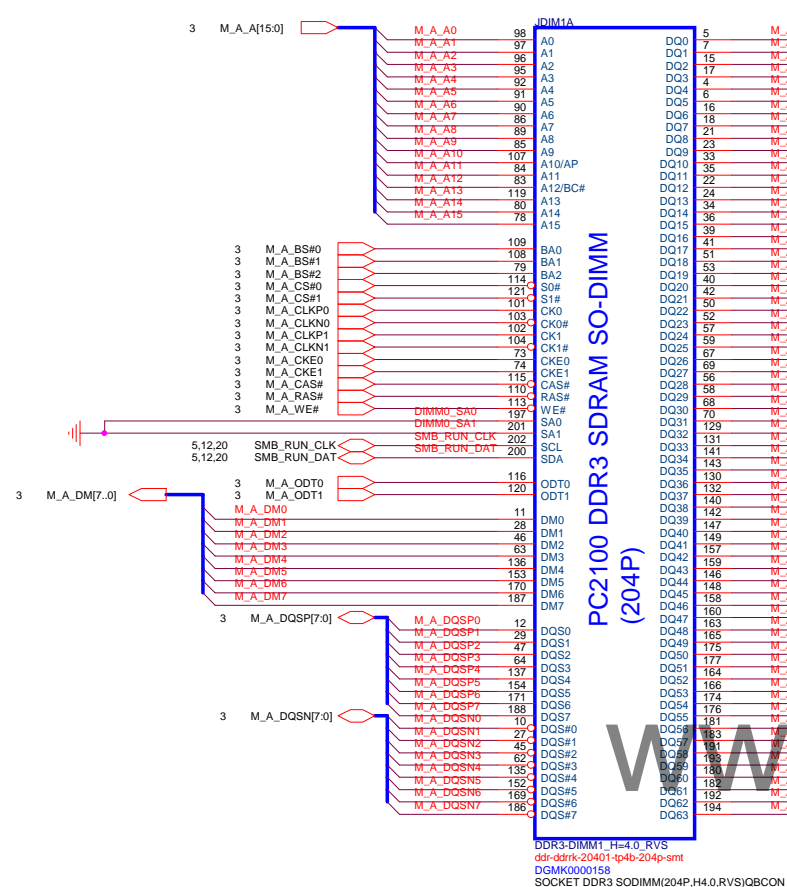


PROJECT : X21
Quanta Computer Inc.

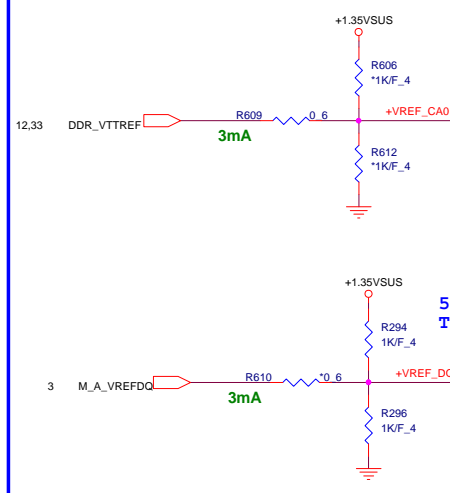
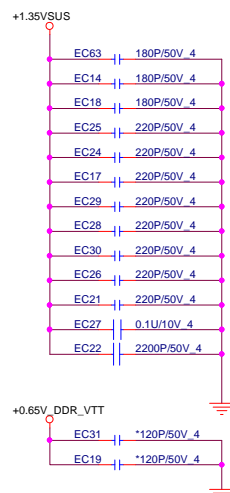
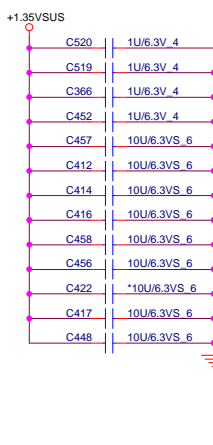
Size	Document Number	Rev
	Carrzio 7/7 (GND)	1A
Date: Friday, October 17, 2014	Sheet	of 43

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Place these Caps near So-Dimm0.

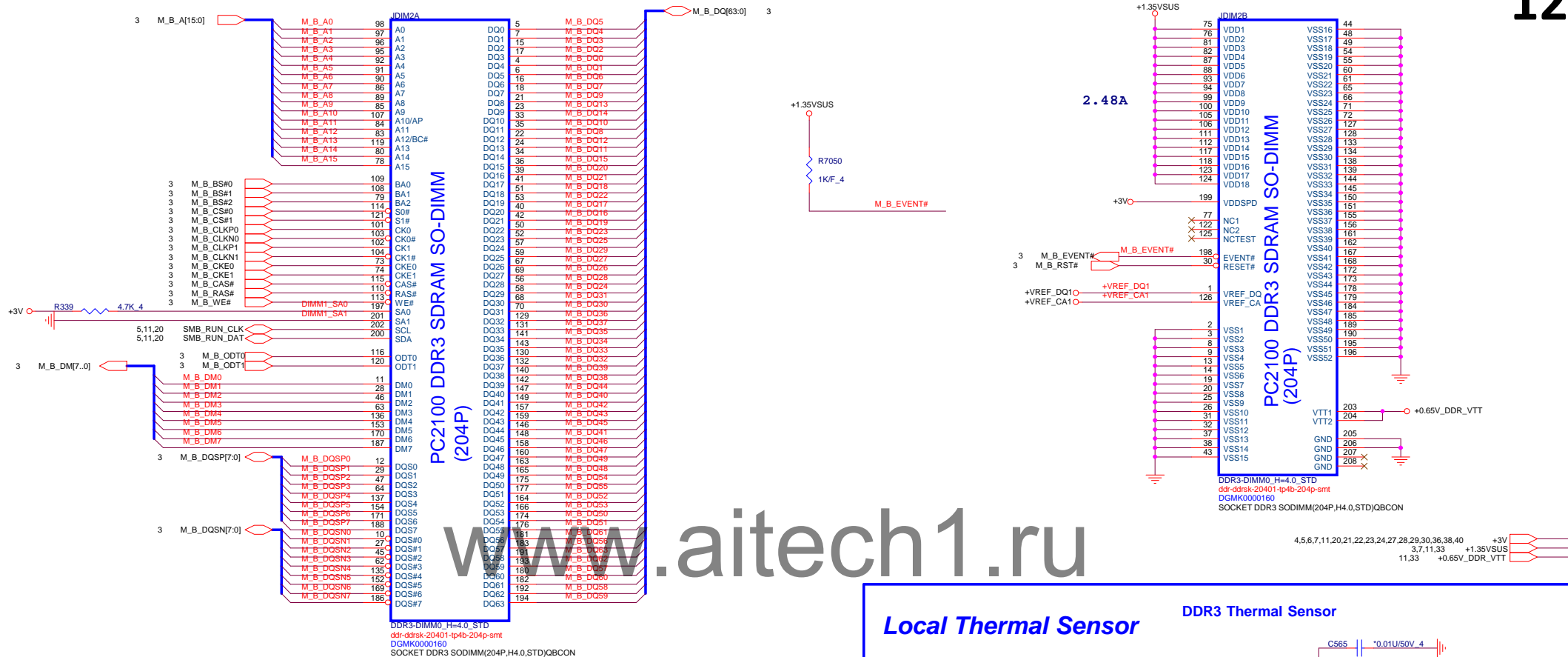


53537_105 change:
Type 1: and Type 2: from 1K/2 voltage



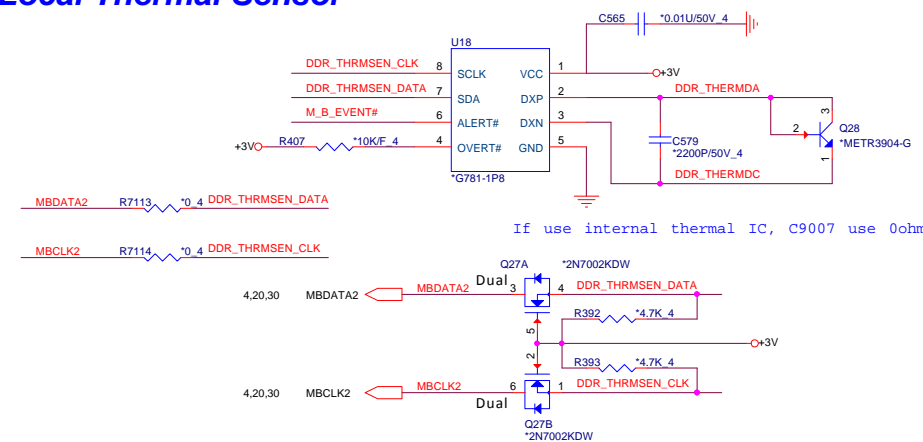
PROJECT : X21
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 1/2 (4H)	1A
Date: Friday, October 17, 2014	Sheet 11 of 43	



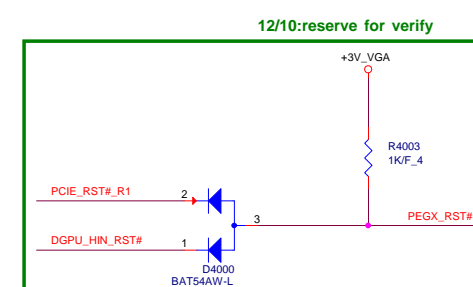
Local Thermal Sensor

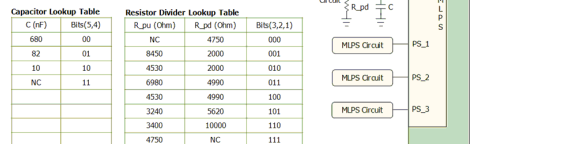
DDR3 Thermal Sensor



Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

PROJECT : X21			
Quanta Computer Inc.			
Size	Document Number	Rev	
Custom	System Memory 2/2 (4H)	1A	
Date: Friday, October 17, 2014	Sheet 12 of 43		

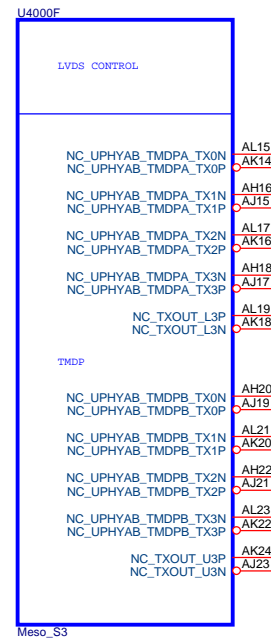
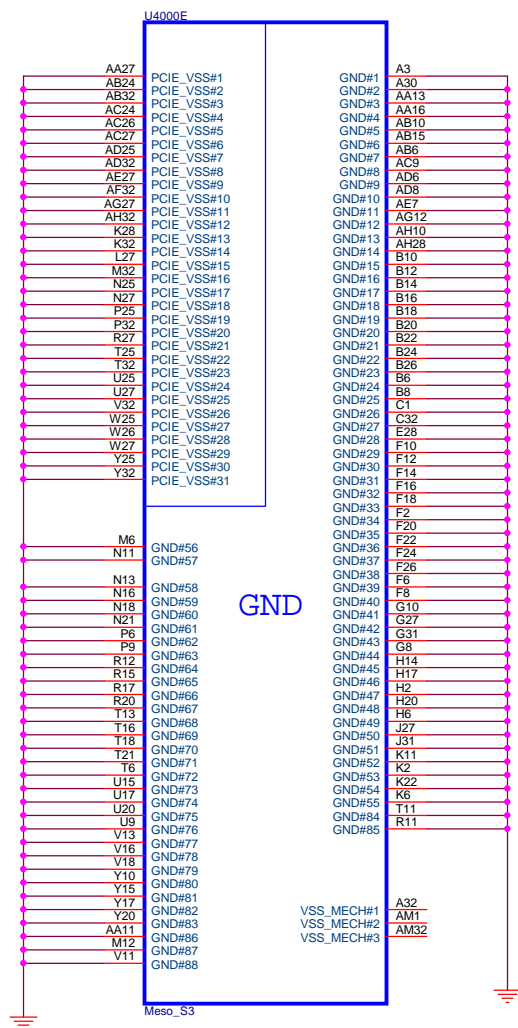




BITS => BIT0	MILPS Bit	Strap Name	Description	Recommended Settings
PS0 => 11001				
PS1 => 11000				
PS2 => 11000				
PS3 => 11000				
	PS_0[1]	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
	PS_0[2]	ROM_CONFIG[1]		
	PS_0[3]	ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[0] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 29).	
	PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
	PS_0[5]	N/A	Reserved.	1
	PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIE GEN3 capability. 1 = PCIE GEN3 is supported. 0 = PCIE GEN3 is not supported.	Design dependent, see the description.
	PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIE reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
	PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
	PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
	PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
	PS_2[1]	N/A	Reserved.	0
	PS_2[2]	N/A	Reserved.	0
	PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
	PS_2[4]	N/A	Reserved.	1
	PS_2[5]	N/A	Reserved.	1
	PS_3[1]	BOARD_CONFIG[0]		
	PS_3[2]	BOARD_CONFIG[1]	Board configuration related strapings, such as for memory ID	Design dependent, see the description.
	PS_3[3]	BOARD_CONFIG[2]		
	PS_3[4]	N/A	Reserved.	1
	PS_3[5]	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	FU	PD
000	Hylix	256Mx16 *4, 900MHz	H5TC4663CFR-N0C	NC	4.75K
001	Samsung	256Mx16 *4, 900MHz	K1W4G1641E-BCLA	8.45K	2K
010	Micron	256Mx16 *4, 900MHz	MT41J256M16A-093G:E	4.53K	2K
011					
100					
101					

4.53K	CS24532FB08
4.75K	CS24752FB12
8.45K	CS28452FB12
2K	CS22002FB19



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

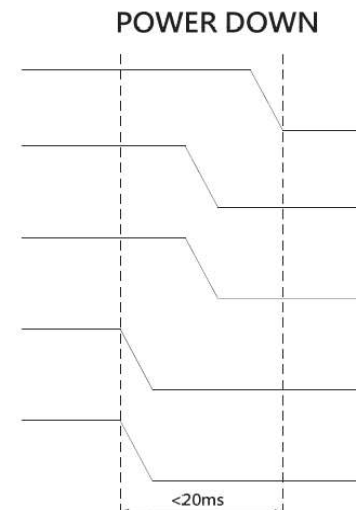
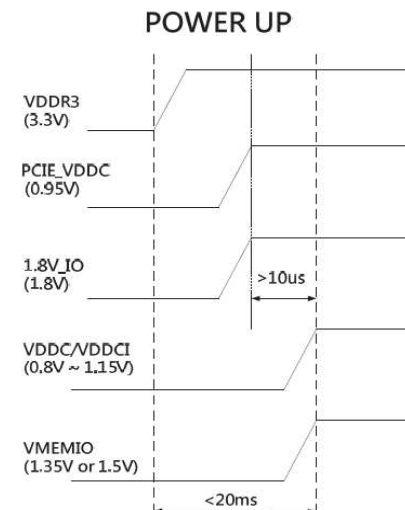
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	x
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

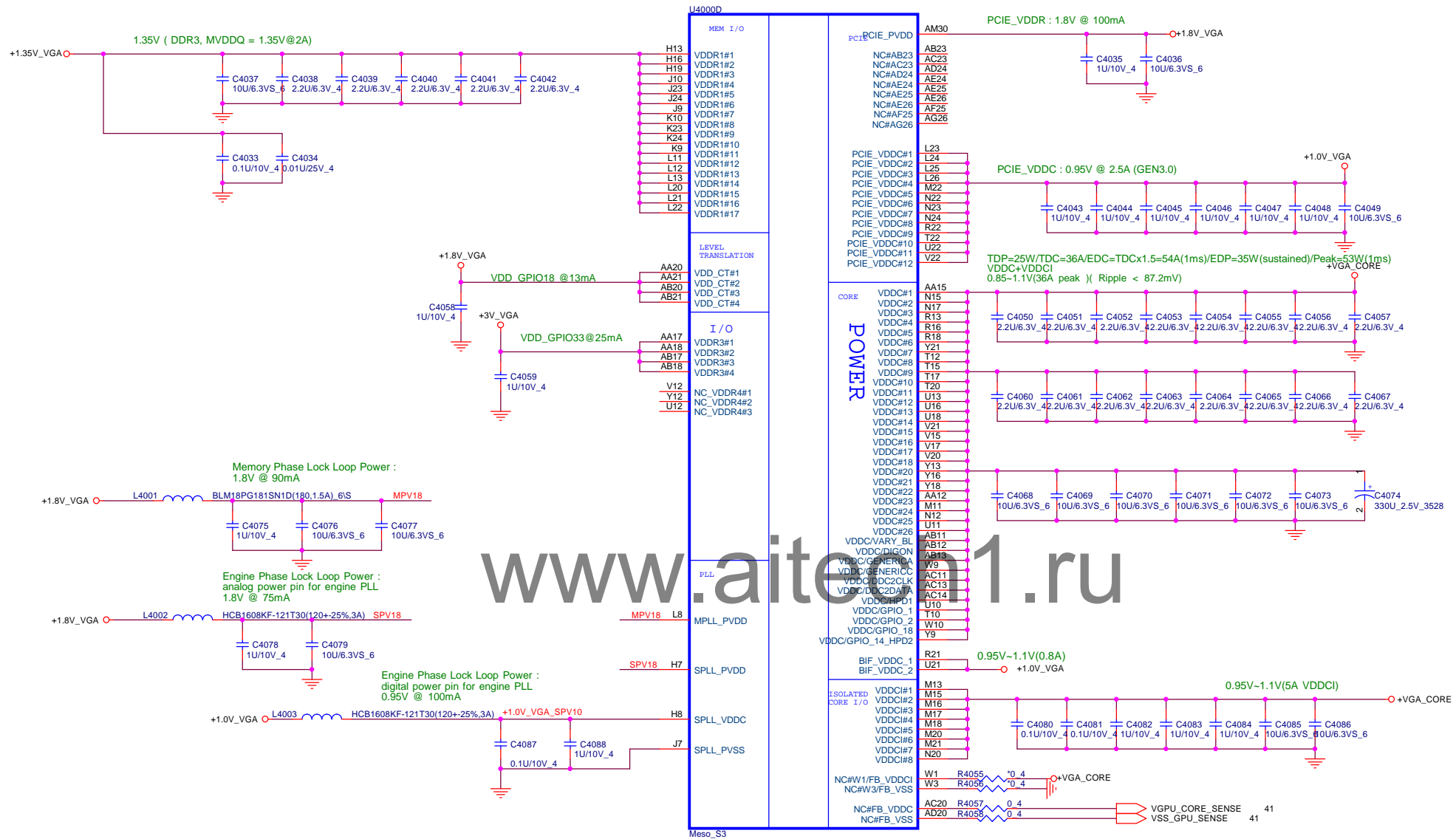
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE



PROJECT : Y23
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date:	Friday, October 17, 2014	Sheet 15 of 43

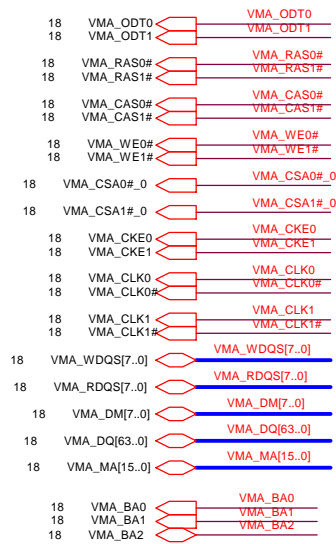


+1.35V_VGA 17,18,40,41
+1.8V_VGA 13,14,40,41,43
+1.0V_VGA 13,40,43
+VGA_CORE 40,41,42



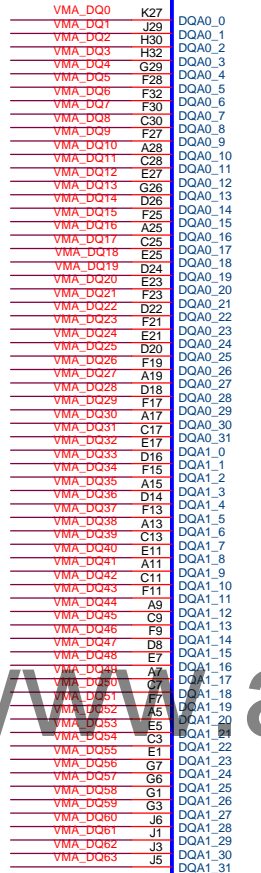
PROJECT : Y23
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ S3 Power	1A
Date:	Friday, October 17, 2014	Sheet 16 of 43

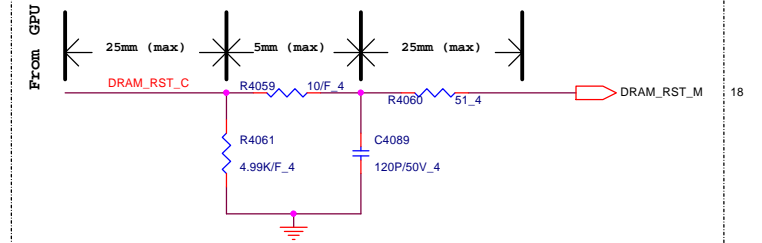
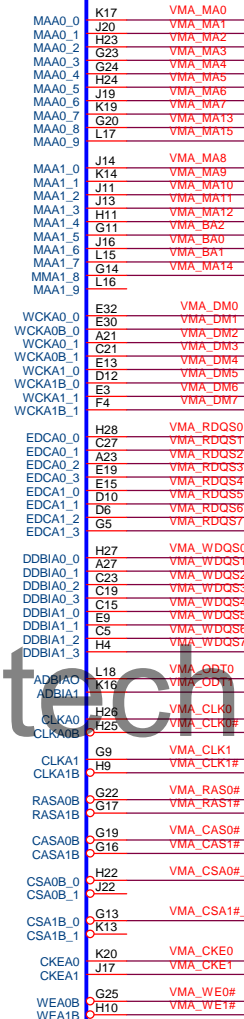


support 1Gbit
VRAM (64M x 16)

U4000C

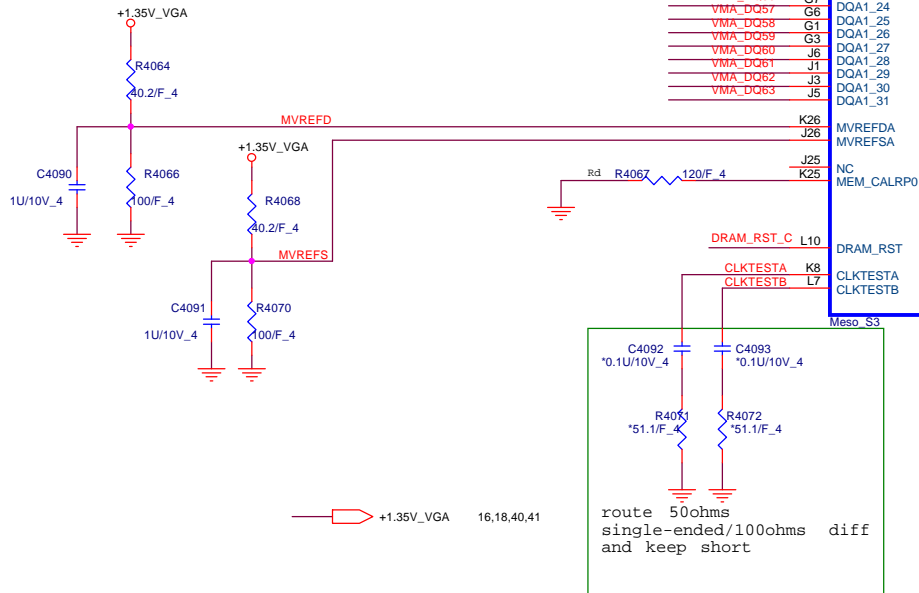


MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

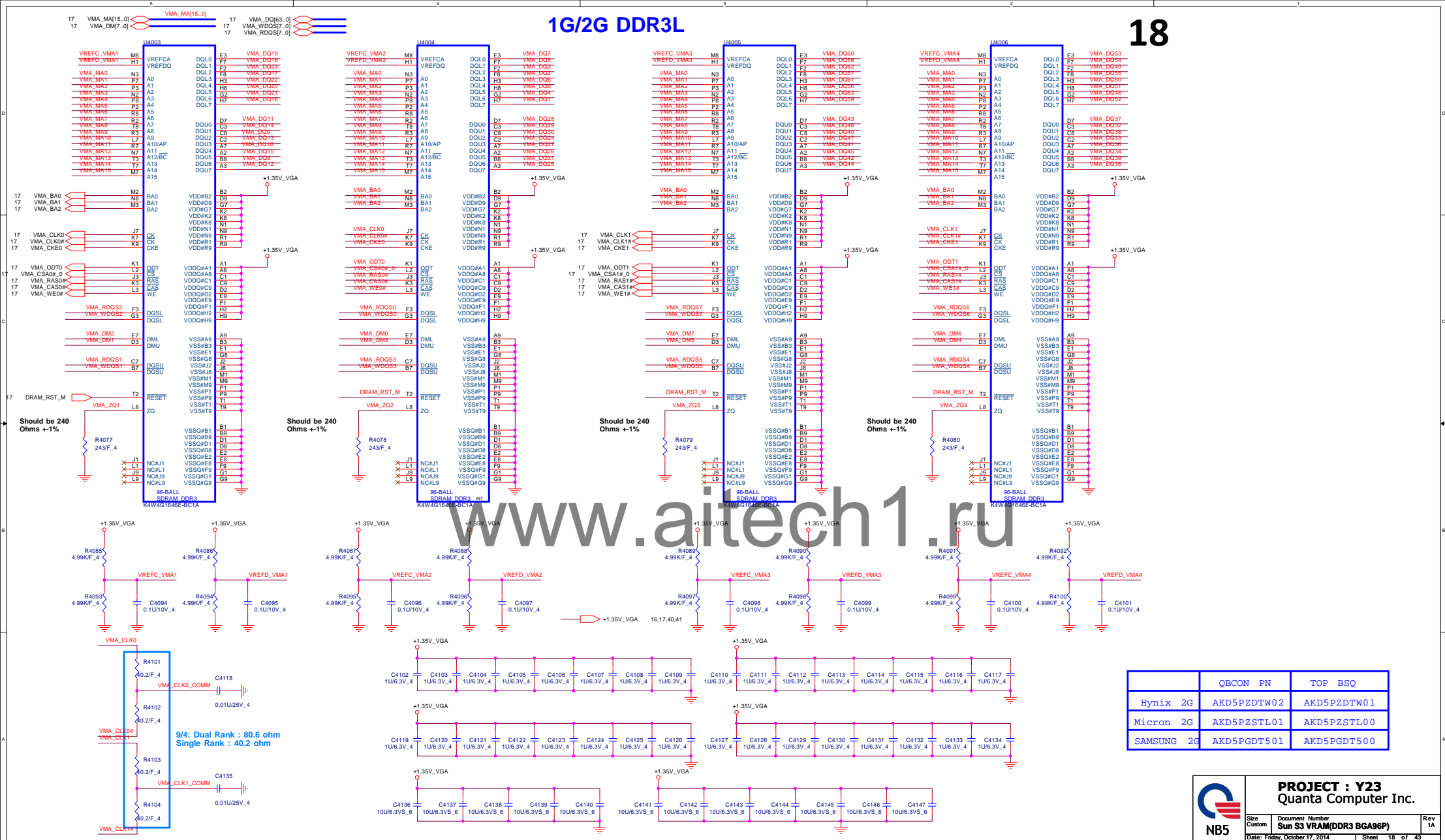


PROJECT : Y23
Quanta Computer Inc.

Size	Document Number	Rev
	TPOAZ_S3_MEM_Interface	1A
Date:	Friday, October 17, 2014	Sheet 17 of 43

1G/2G DDR3L

18



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NB5

PROJECT : Y23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A
Date: Friday, October 17, 2014		Sheet 19 of 43

keep 80 Mile Trace

Top Diagram (L6001):

- Input: +3V
- Regulator: L6001, PB160808T-600Y-N(60.3A), USING 60R 1A
- Output: +TRAVIS3.3V
- Capacitors: C6009 (*100U/6.3VS_6), C6010 (*0.1U/10V_4), C6011 (*0.1U/10V_4), C6004 (*0.1U/10V_4), C6005 (*22U/6.3VS_6)
- Placement: CLOSE TO Pin22, Close to Pin18 within 200-mil

Middle Diagram (L6000):


- Input: +3V
- Regulator: L6002, PB160808T-600Y-N(60.3A)
- Output: +TRAVIS3.3V_A
- Capacitors: C6006 (*100U/6.3VS_6), C6007 (*0.1U/10V_4), C6008 (*0.1U/10V_4)
- Placement: Close to Pin5

Bottom Diagram (L6000):

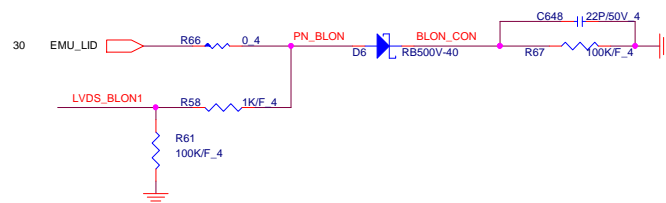
- Input: SWR_LX
- Regulator: L6000, *4.7UH20%.0.76ALVF303010-4R7M-N
- Output: +TRAVIS1.2V
- Capacitors: C6001 (*100U/6.3VS_6), C6002 (*0.1U/10V_4), C6003 (*0.1U/10V_4), C6000 (*0.1U/10V_4)
- Resistor: R6008 (*0.8)
- Placement: Close to Pin17, Close to Pin43, Close to Pin11
- SWR: Stuff L6000
- LDO: Stuff R6008 (default pop this)

Legend:

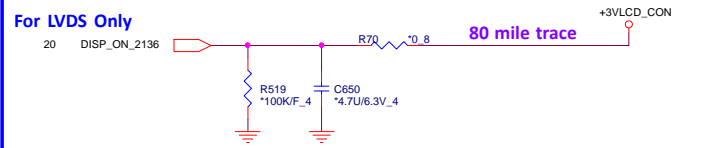
- L6000: need use CV-4709MN00 for Vendor suggestion
- 2nd CV-4709MN03

 NB5	PROJECT : X21 Quanta Computer Inc.		
	Size Custom	Document Number LVDS converter RTD2136	Rev 1A
	Date: Friday, October 17, 2014		Sheet 20 of 43

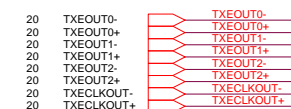
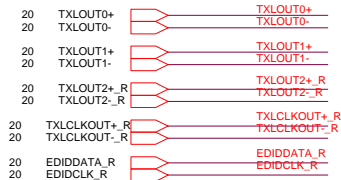
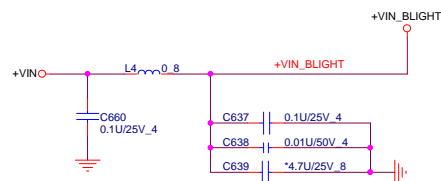
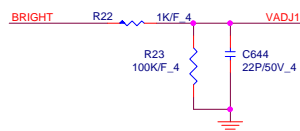
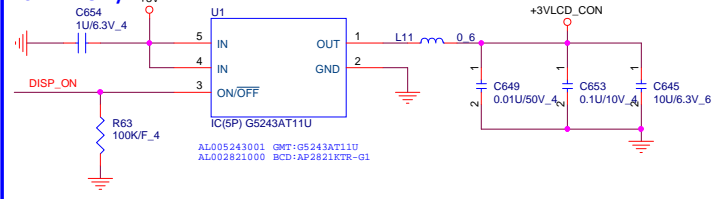
LVDS conn.
14" & 15" only eDP panel SK, 17" have both LVDS & eDP SK



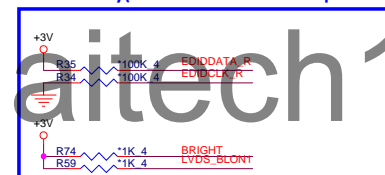
For LVDS Only



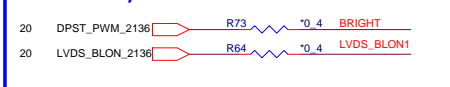
For EDP Only



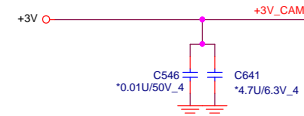
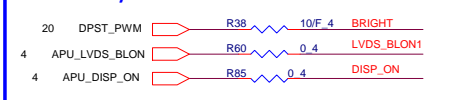
For EDP Only (DG show AUX don't require PU/D)



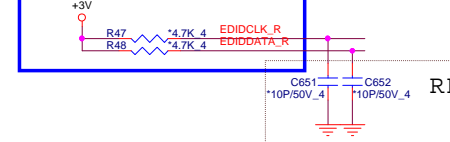
For LVDS Only



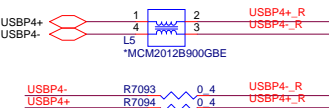
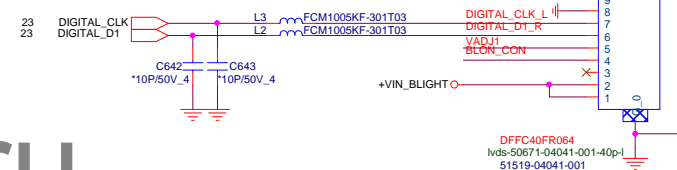
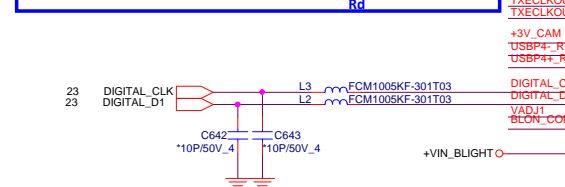
For EDP Only



For LVDS

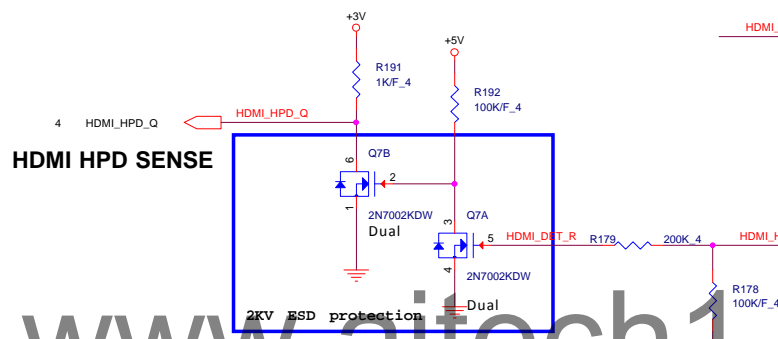
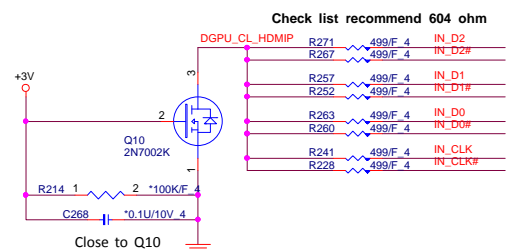
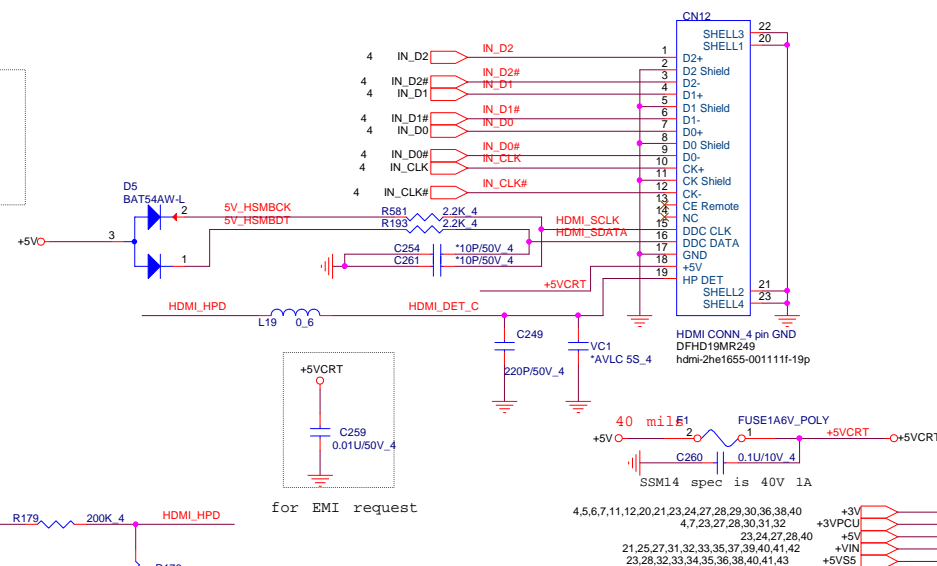
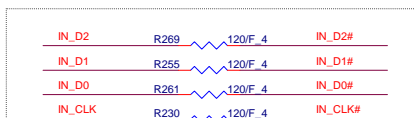


For LVDS Only: Stuf f Rc For EDP Only: Stuf f Rd

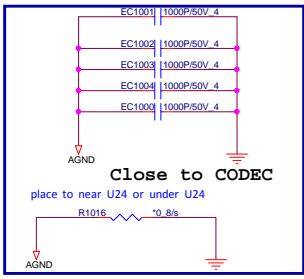


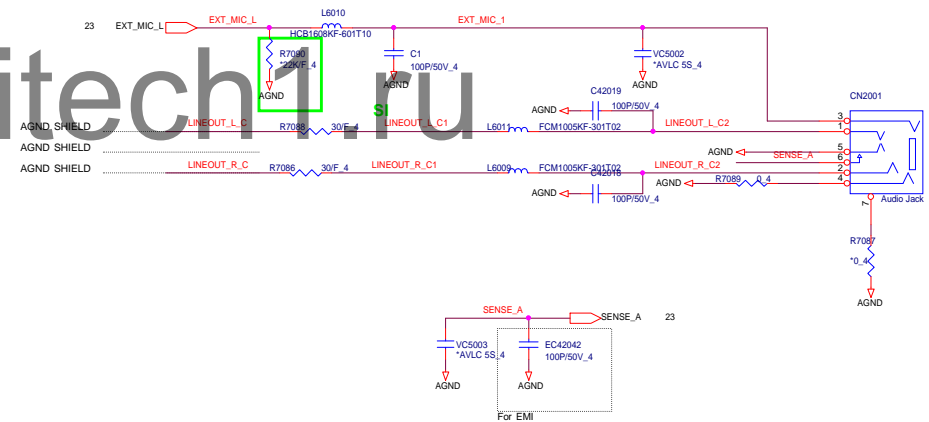
4,5,6,7,11,12,20,22,23,24,27,28,29,30,36,38,40
25,27,31,32,33,35,37,39,40,41,42

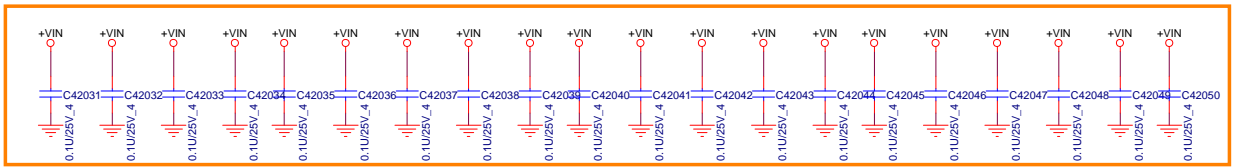
Close to HDMI connector



for EMI request

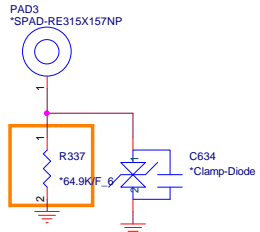
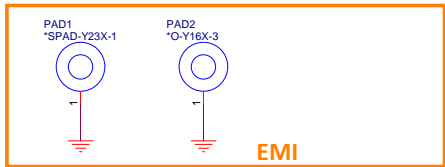
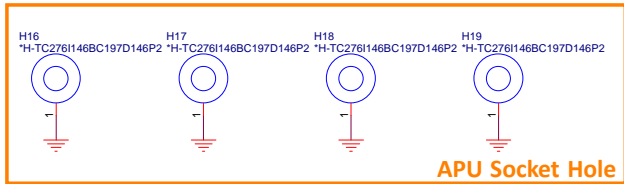
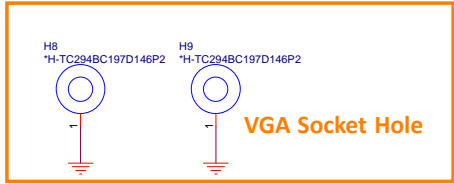




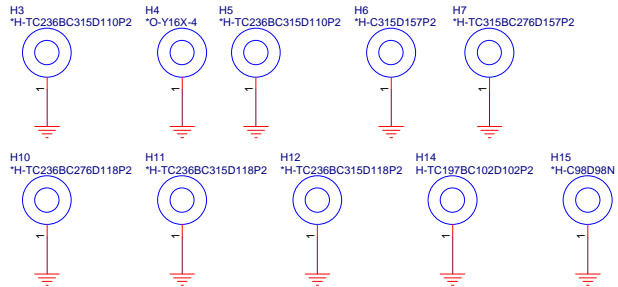


Place on 19V path

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R: 64.9K, NC first



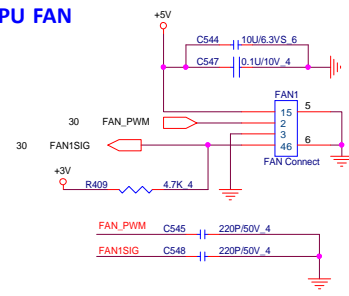
Nut for WLAN

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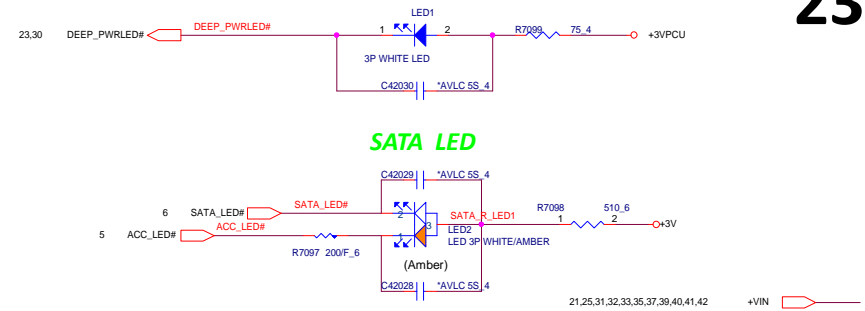
 NB5	PROJECT : X21 Quanta Computer Inc.		
	Size Custom	Document Number AMP TPA6130A2	Rev 1A
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Power But t on Connect or (movet o DB)

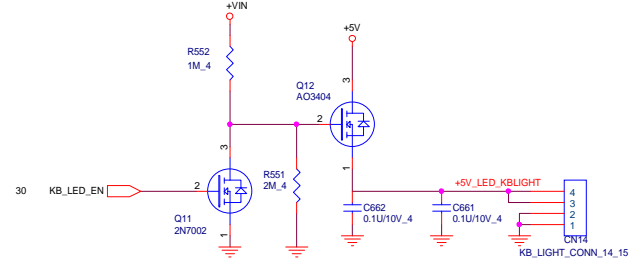
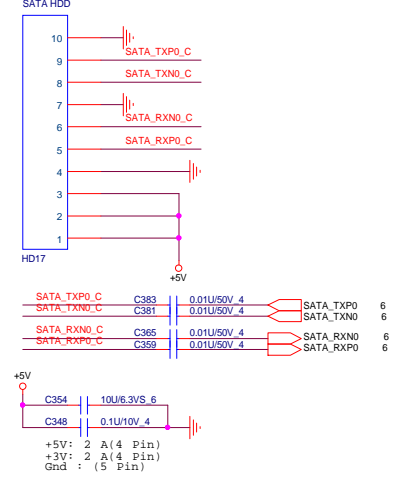
CPU FAN



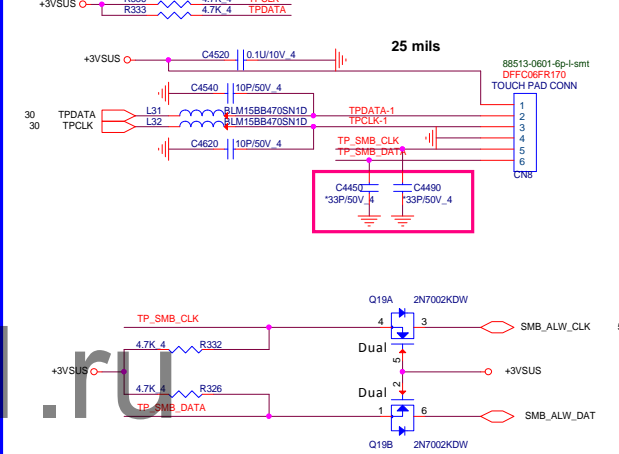
PWR LED



SATA HDD Connector(Cable type)

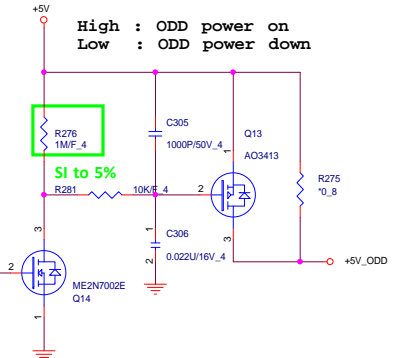
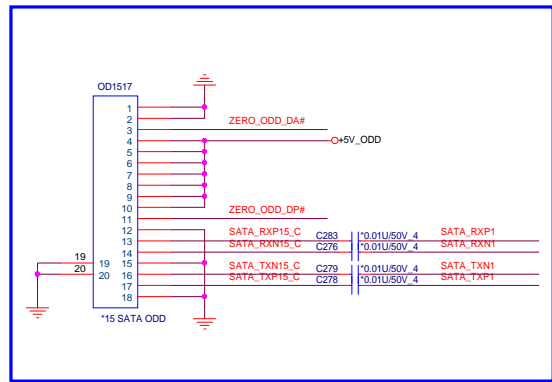
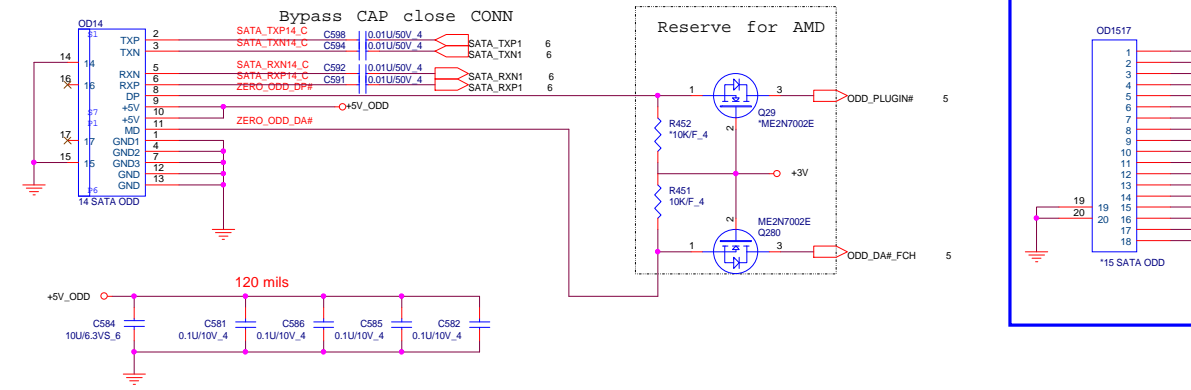


Touch Pad

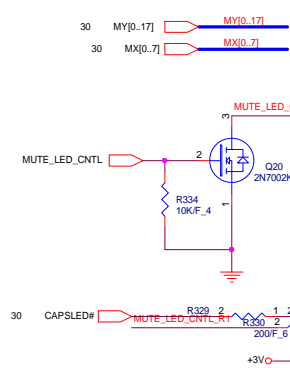


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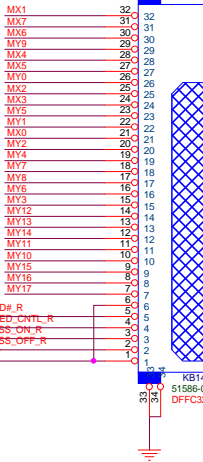
SATA ODD CONNECTOR



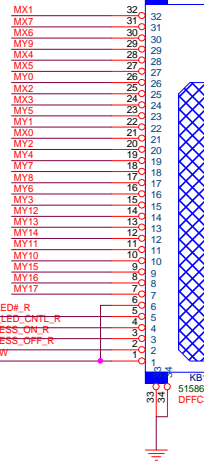
KEYBOARD Con.



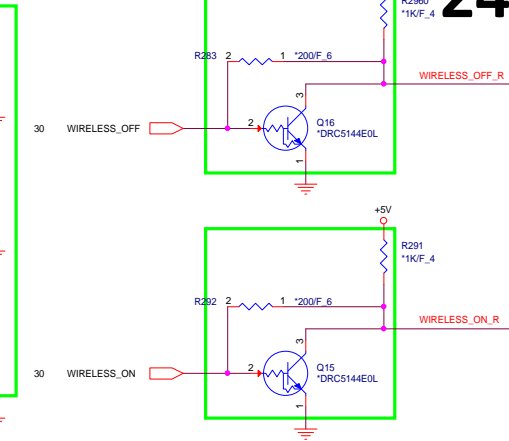
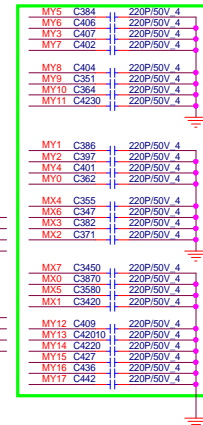
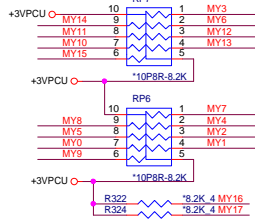
KB 14" & 15"



KB 17"

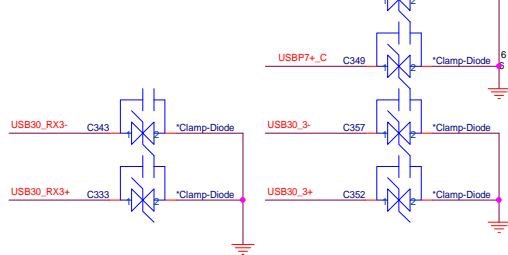


KEYBOARD PULL-UP

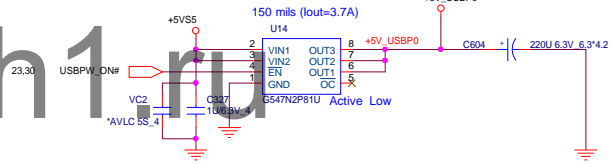
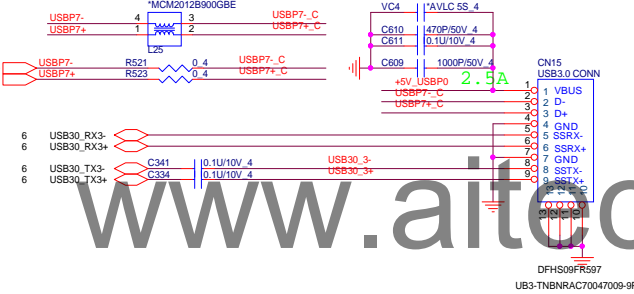


24

USB 2.0/3.0 Combo



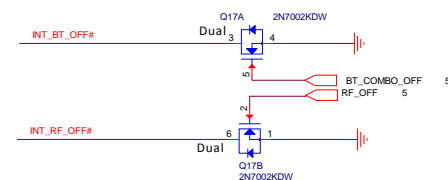
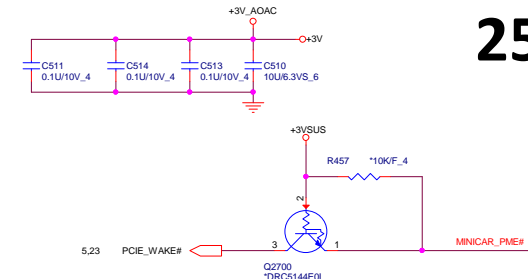
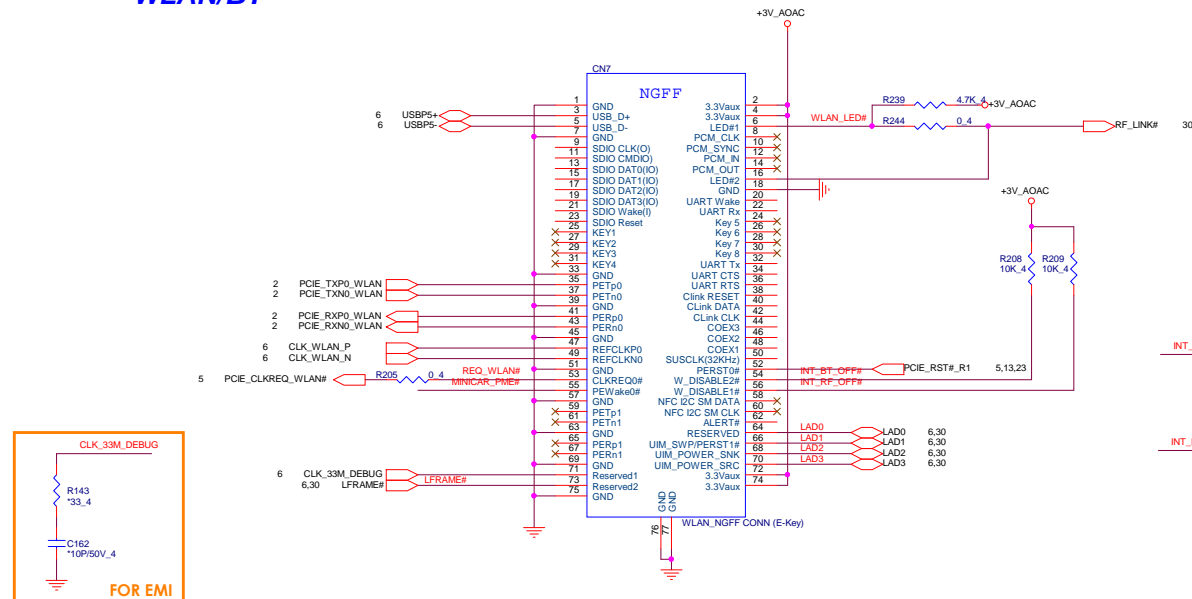
EMI: if charger IC no use, pop this choke



23,32,33,34,35,36,38,40,41,43
4,7,23,27,30,31,32

+5V/S5
+3VPCU

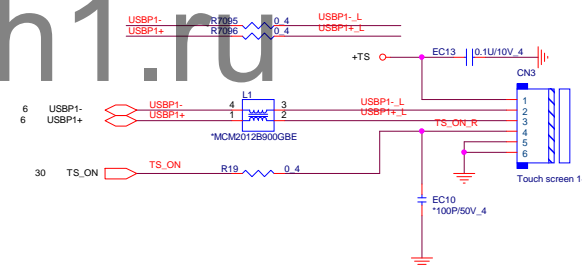
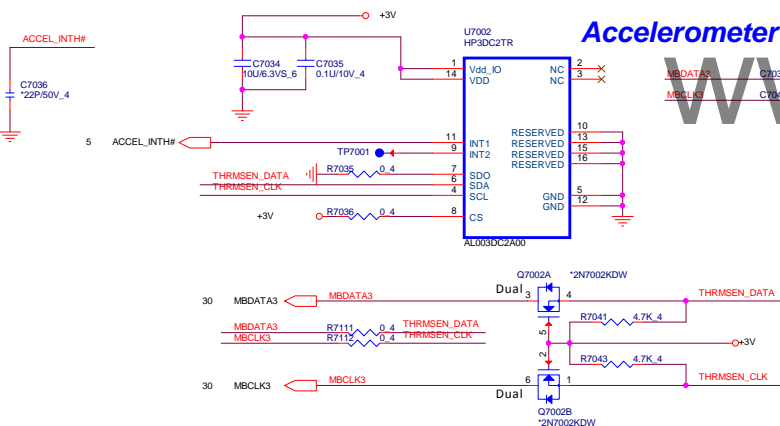
WLAN/BT



Accelerometer Sensor

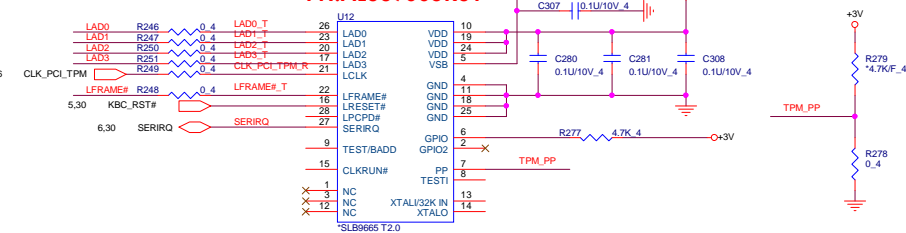
Touch screen

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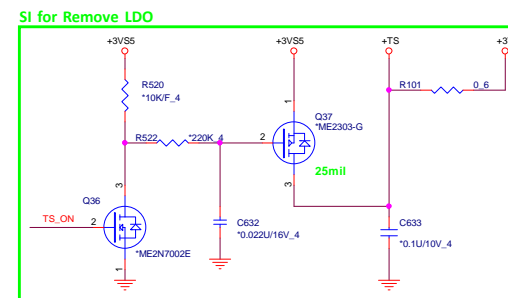


TPM (2.0)

PN:AL009665K01

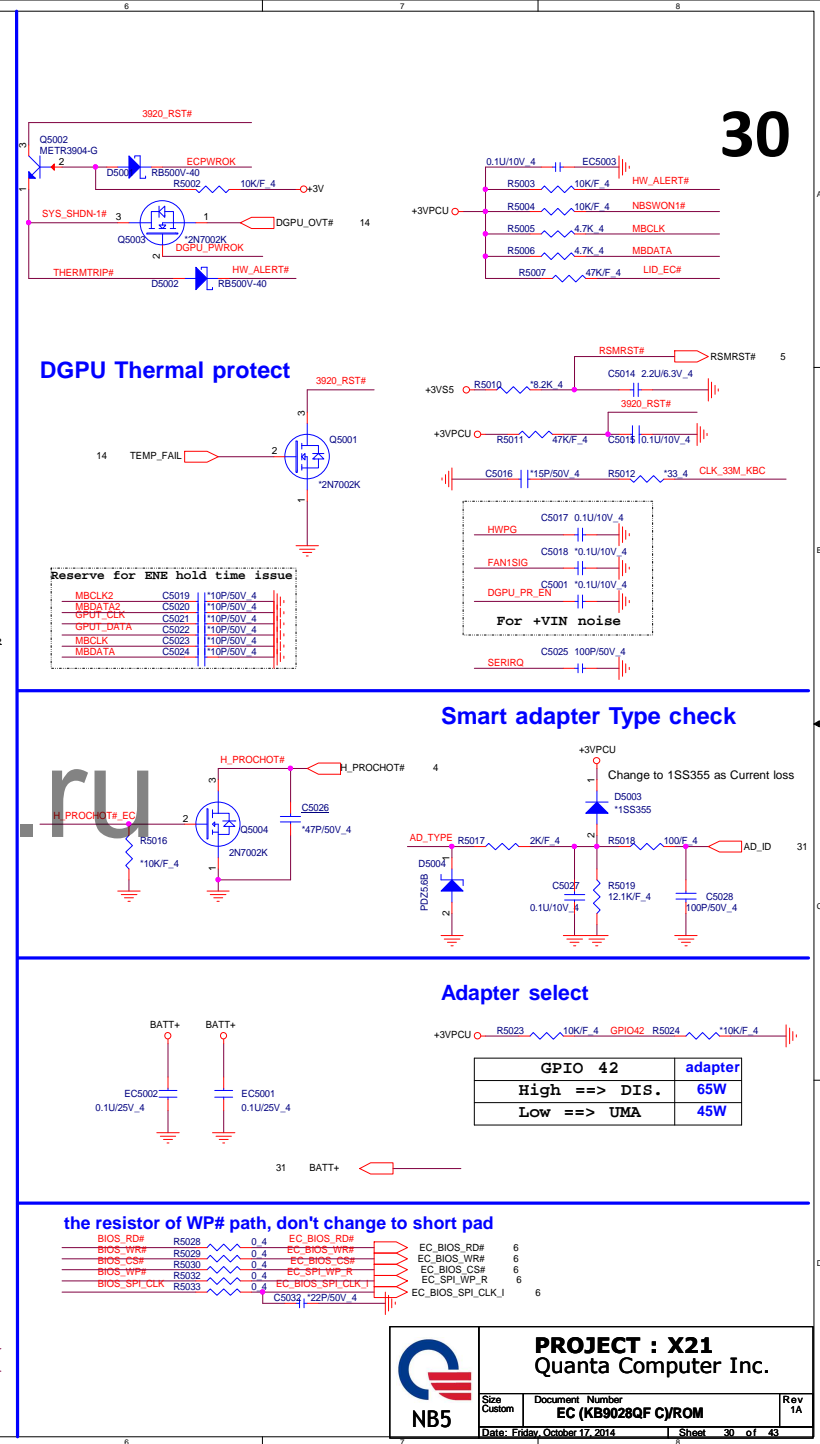
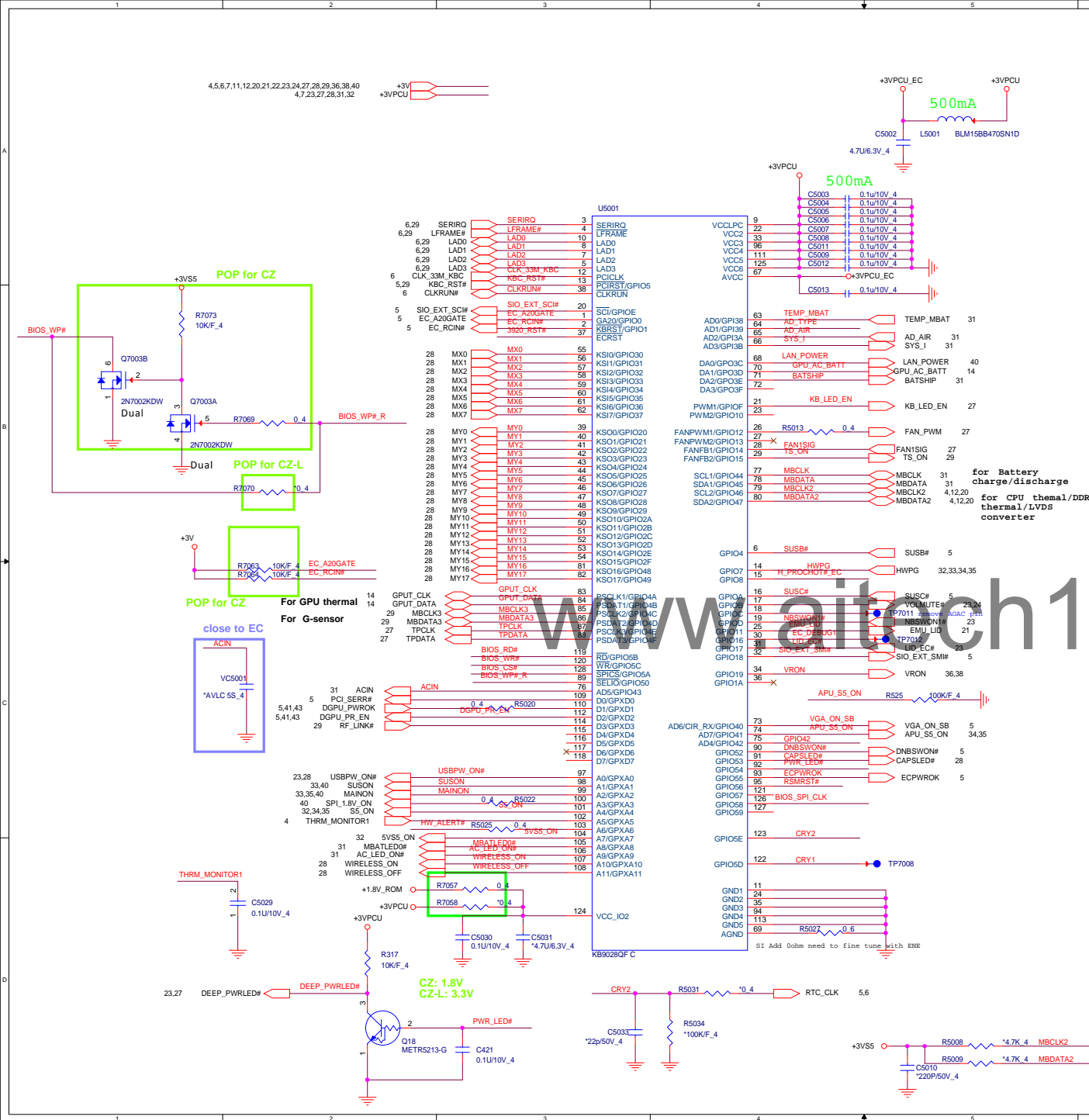


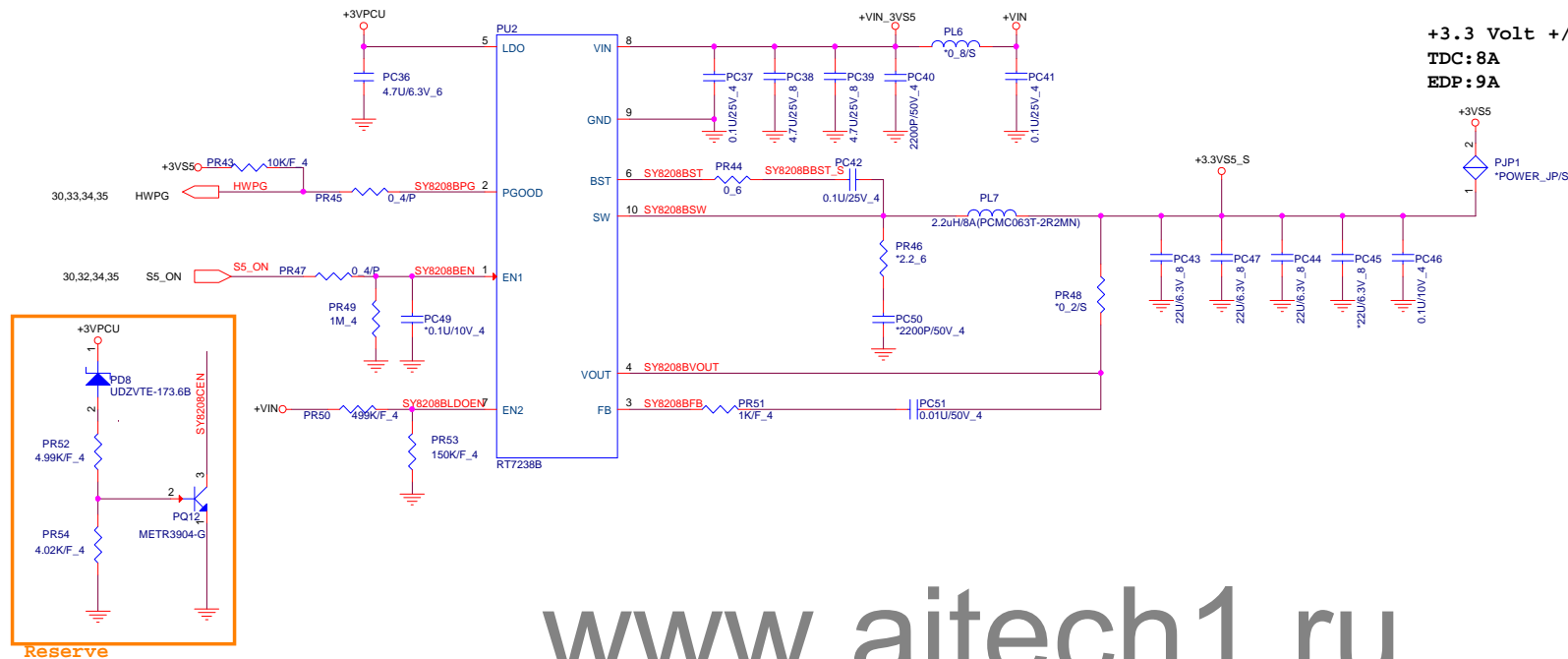
5,6,7,30,32,34,40,41,43
4,5,6,7,11,12,20,21,22,23,24,27,28,30,36,38,40
4,7,23,27,28,30,31,32



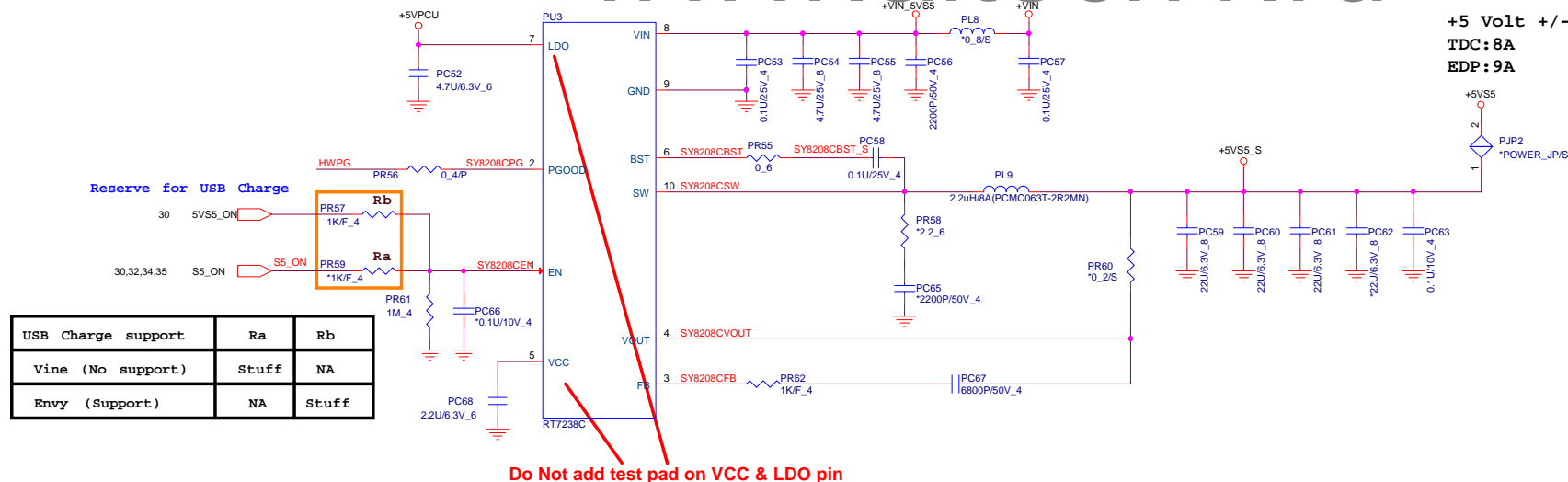
PROJECT : X21
Quanta Computer Inc.

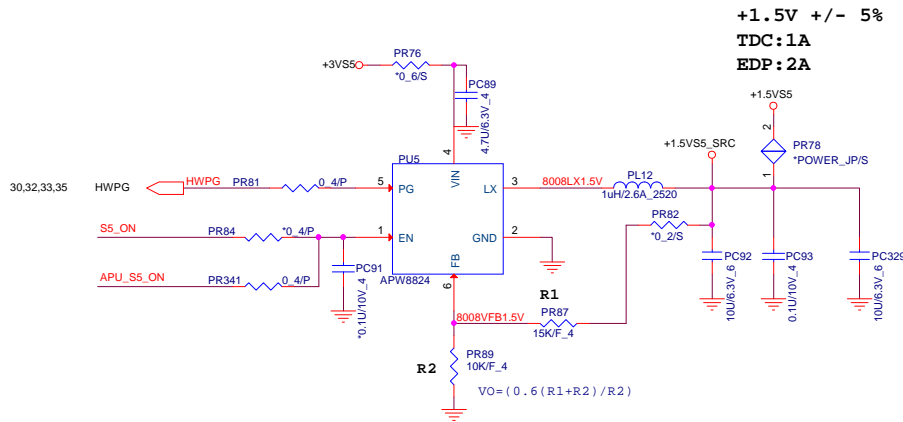
Size Custom	Document Number	Rev 1A
	WLAN/G-Sensor/GCLK/TPM	
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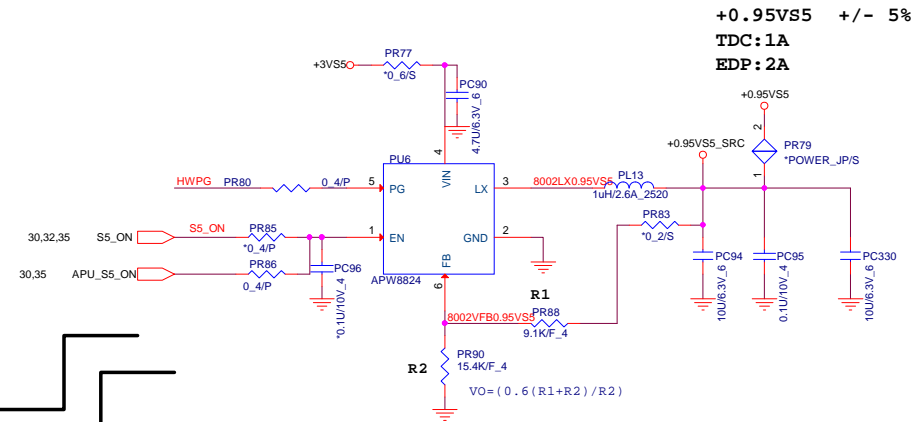
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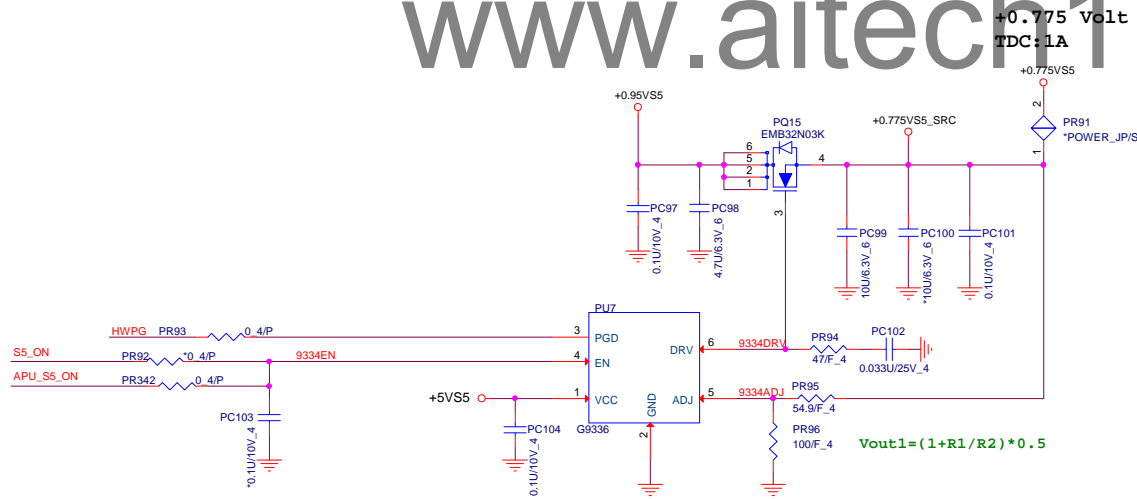


S5_ON

APU_S5_ON



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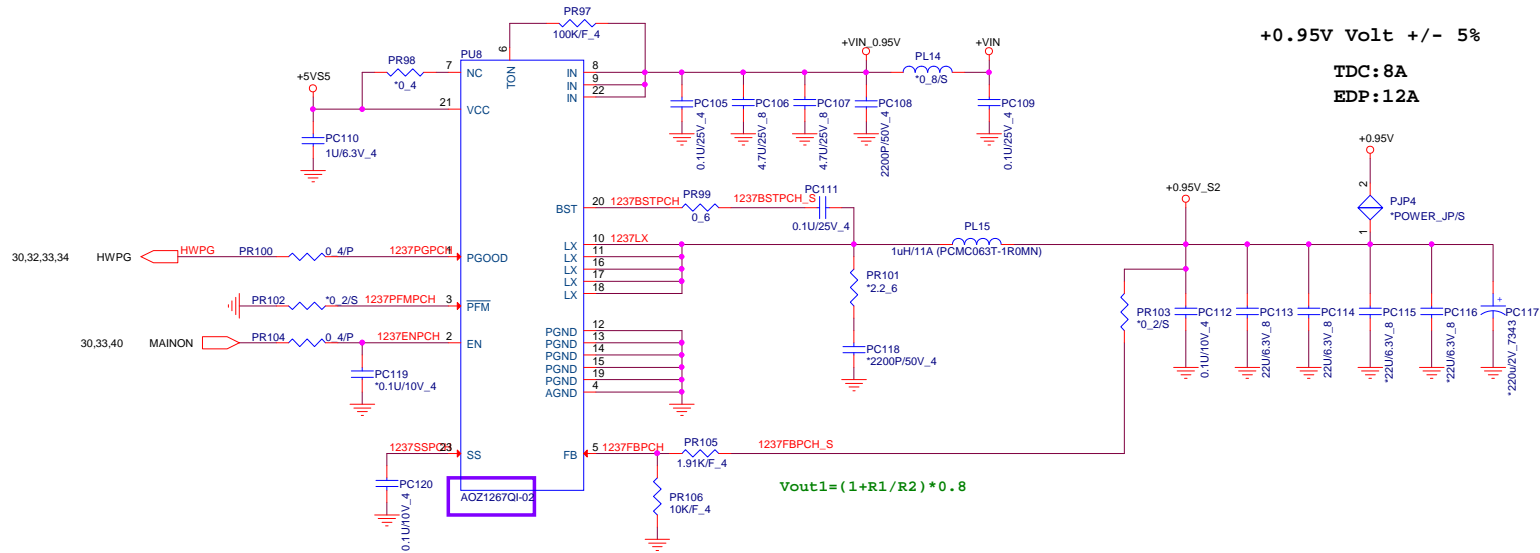


+VIN 21,25,27,31,32,33,35,37,39,40,41,42
+3VS5 5,6,7,29,30,32,40,41,43
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+5VPCU 31,32



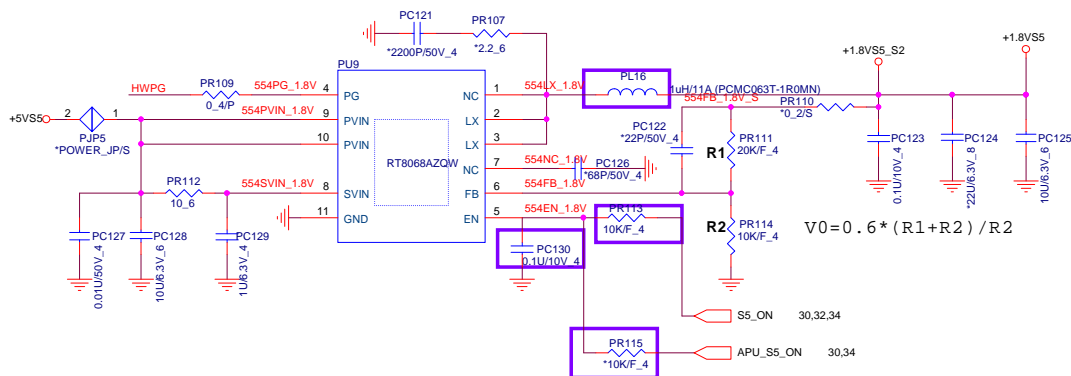
PROJECT : X21
Quanta Computer Inc.

Size Custom	Document Number +1.1VS5 (RT8228)/2.5V	Rev 1A
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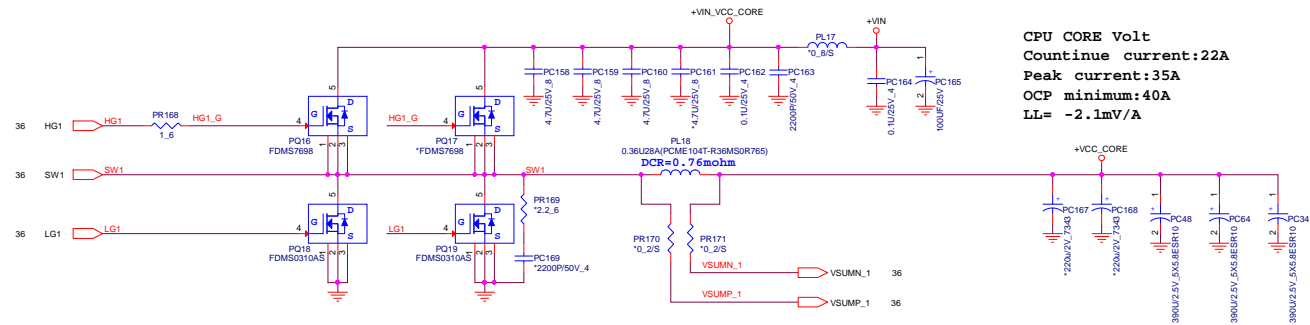
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1.8VS5 +/- 3%
TDC: 3A
EDP: 4A

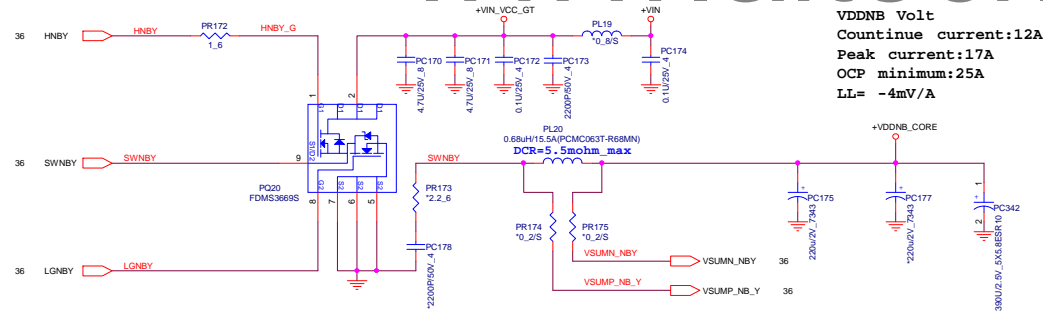


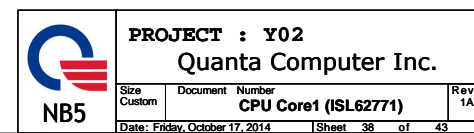
PROJECT : X21
Quanta Computer Inc.

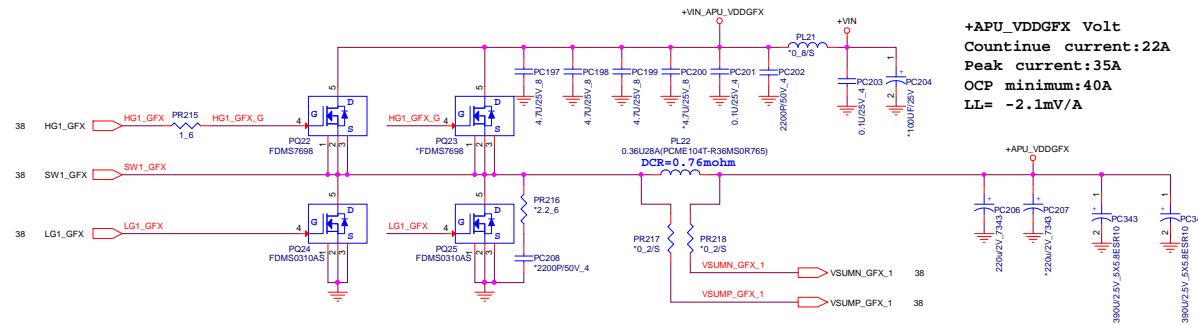
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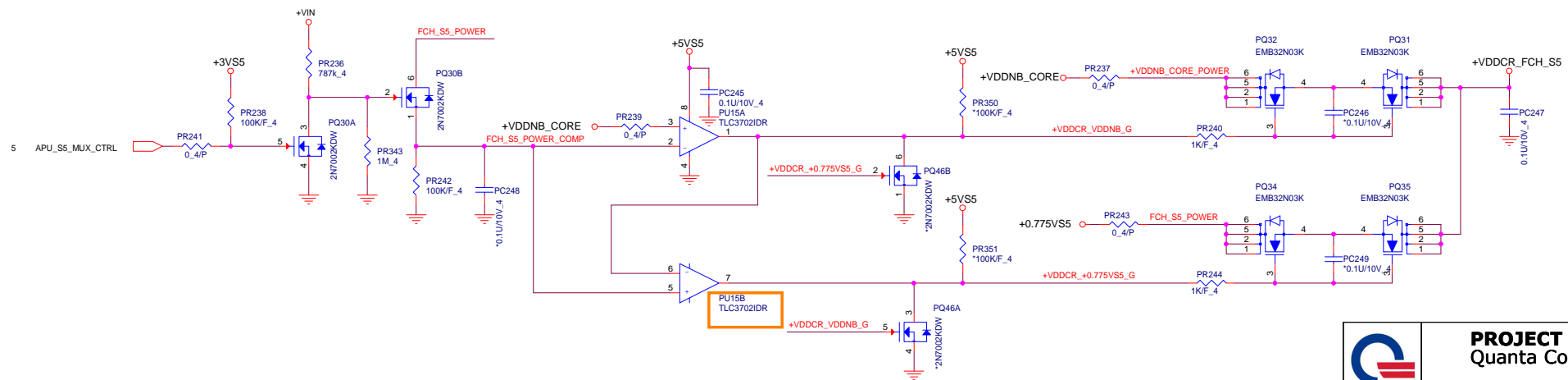
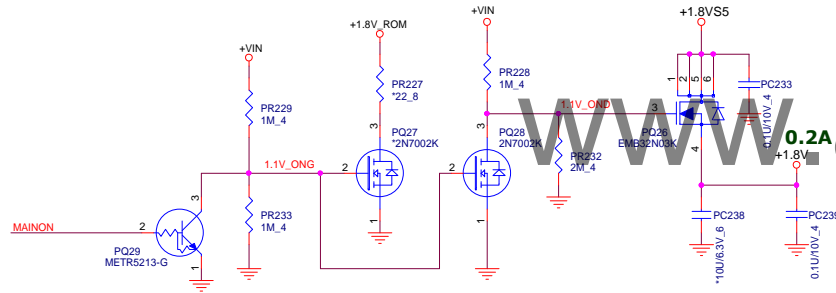
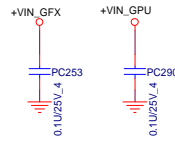
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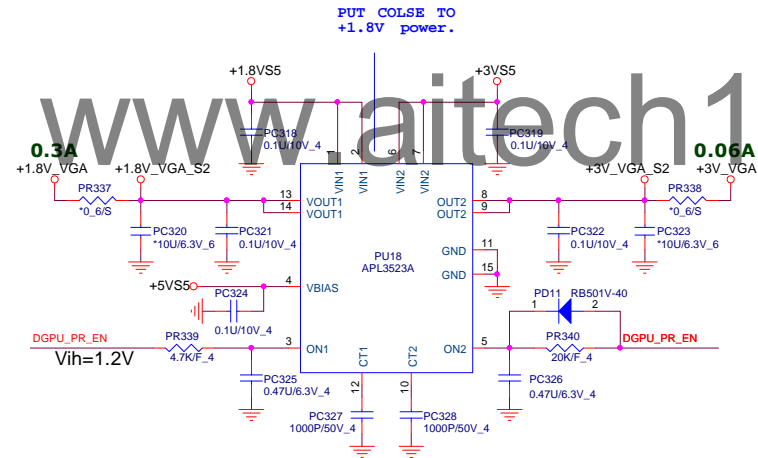
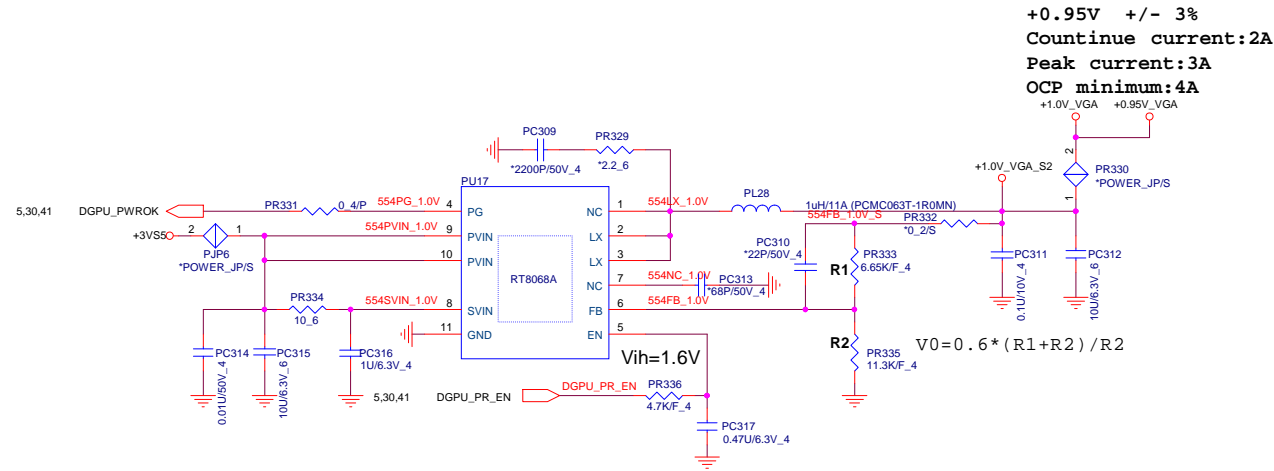






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+3V_VGA

+1.8V_VGA & +0.95V_VGA

+VGA_CORE & +1.35_VGA



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